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Fast and Accurate RF component characterization enabled by FPGA technology

Guillaume Paillonc y

Senior Systems Engineer

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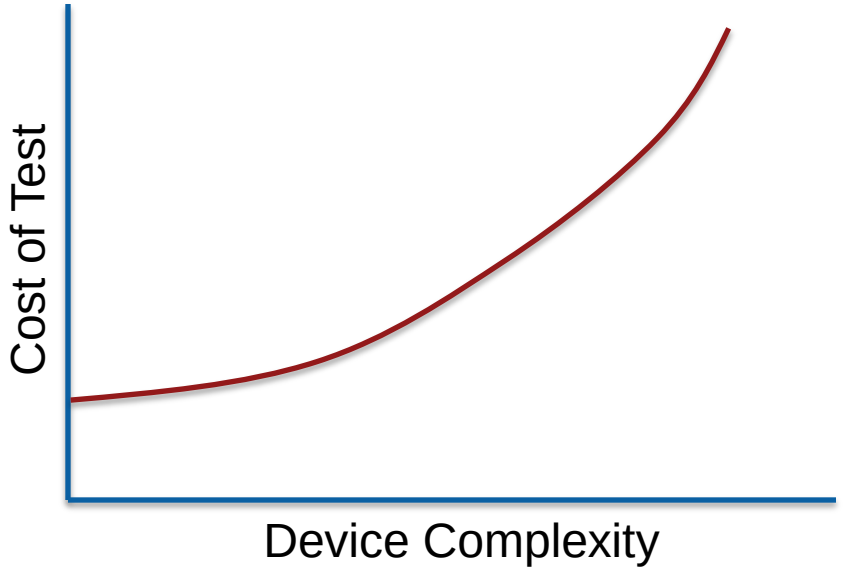
Agenda

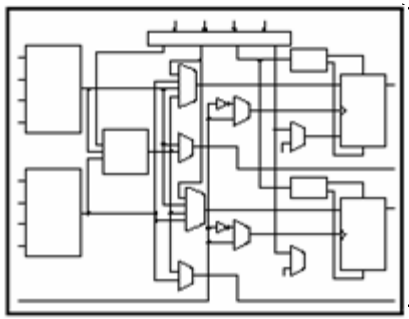
- RF Application Challenges
- What are FPGAs and why are they useful?
- FPGA-based Applications
  - PA Power Leveling
  - Fast Characterization under non-50Ohm
- Conclusions

RF Application Challenges

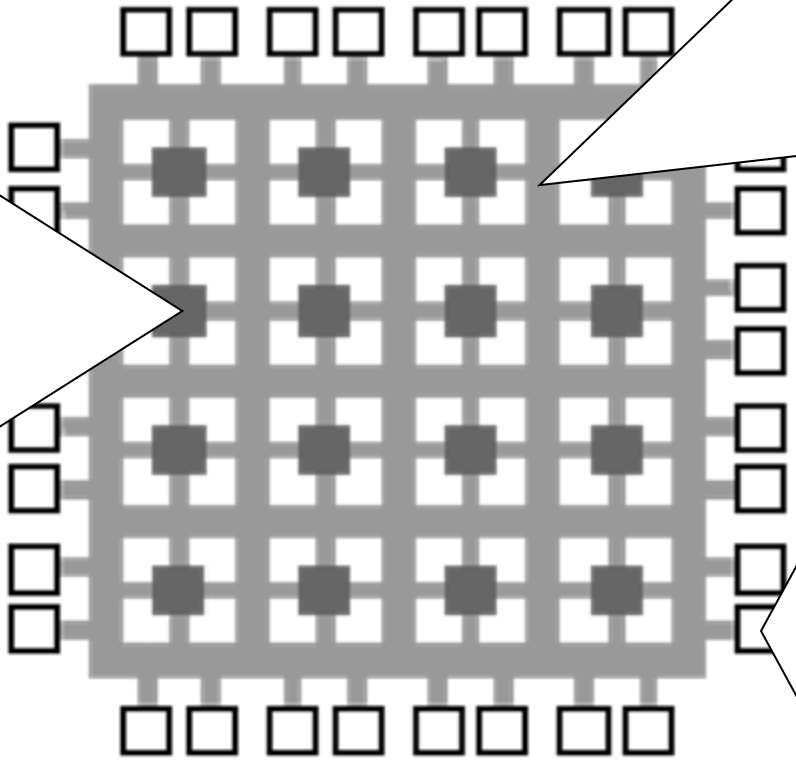
- **Cost of Test**
  - Rapidly Changing RF Standards (802.11ac, LTE)
  - More RF Complexity in Mobile Devices
  - Increasing Test Time
- **Need for Customization**
  - Integrated DUT Control
  - Custom Triggering
  - Test Sequencing
- **Advanced Applications**
  - Channel Emulation
  - Software-Defined Radio
  - Power Level Servoing

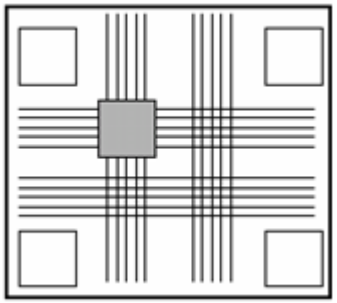


FPGA Technology

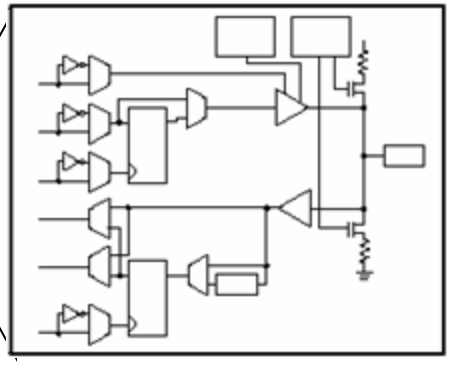


Logic Blocks





Programmable Interconnects

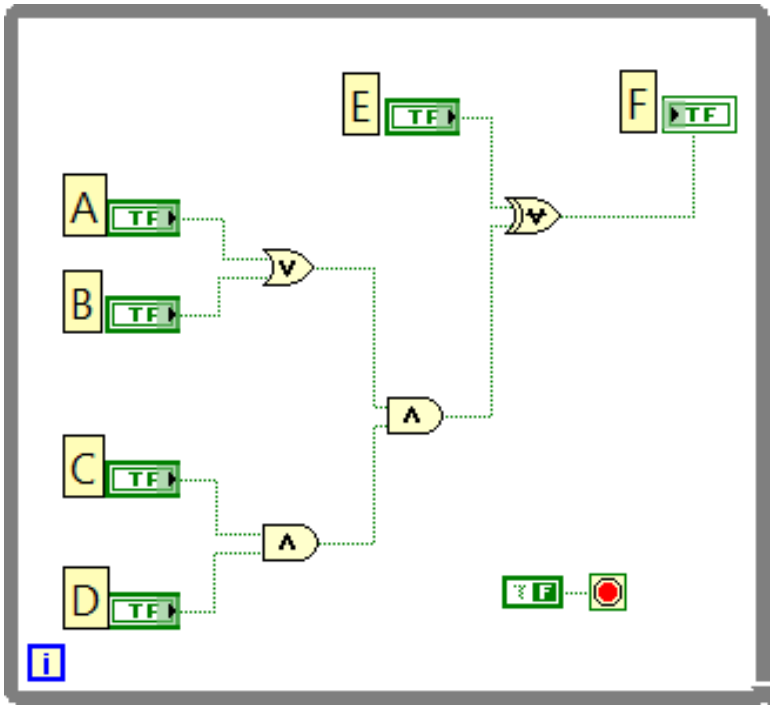


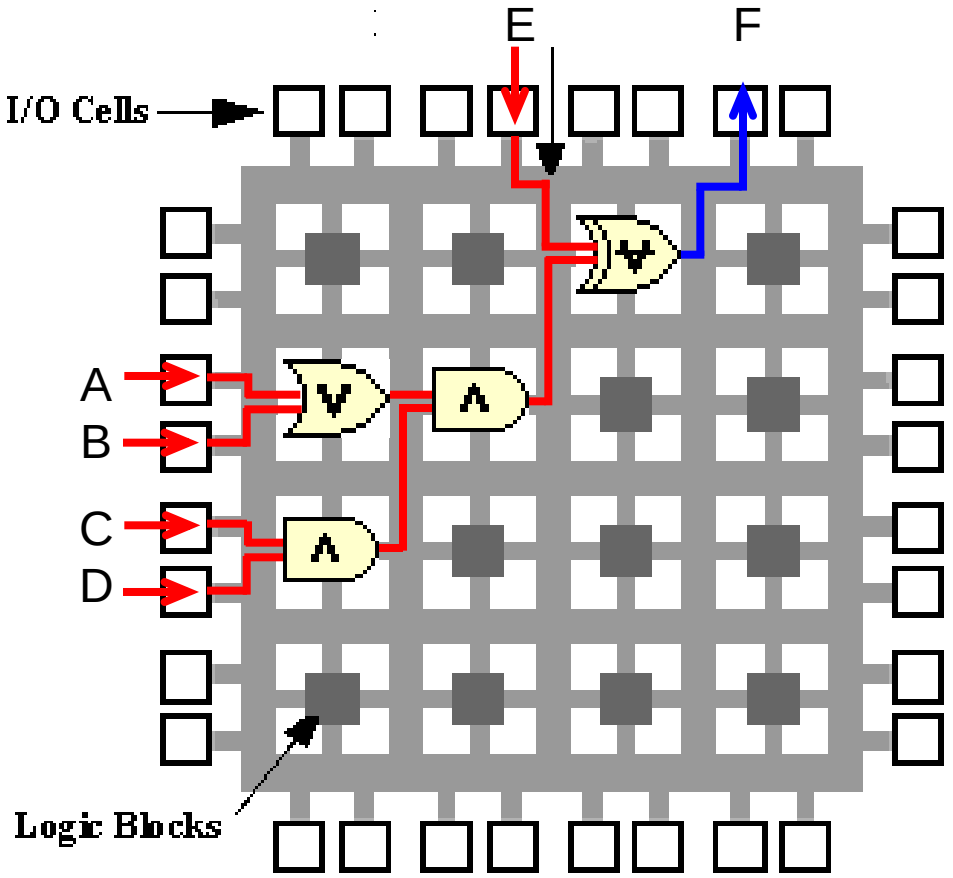
I/O Blocks

FPGA Logic Implementation

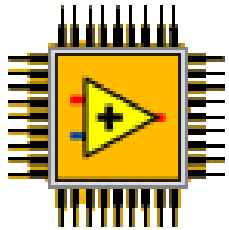
Implementing Logic on FPGA: F = {(A+B)CD} ⊕ E

LabVIEW FPGA Code





Why are FPGAs useful?

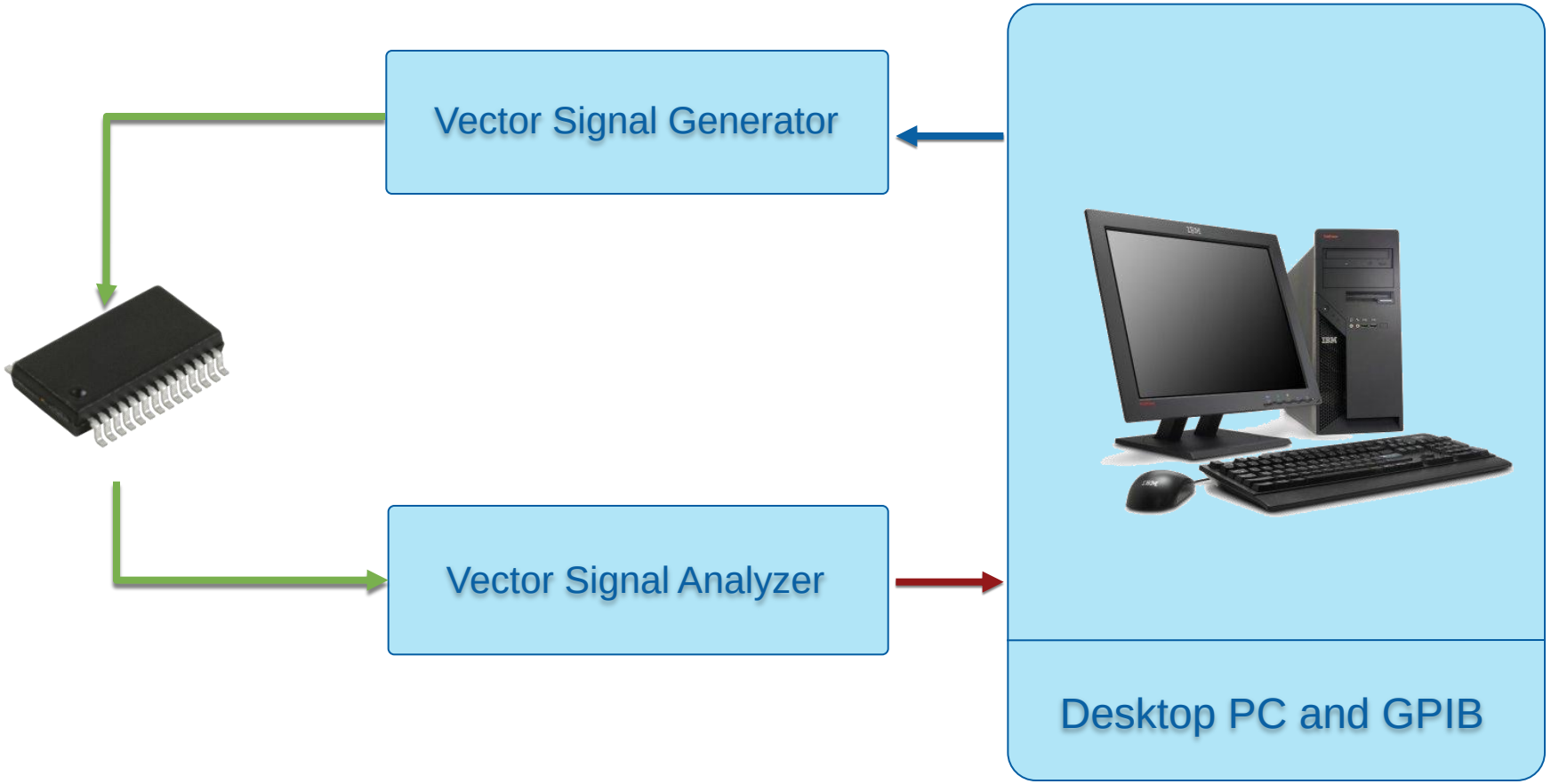


- **High Reliability** – Designs implemented in hardware
- **Low Latency** – Run algorithms at deterministic rates down to 5 ns
- **Reconfigurable** – Create DUT / application-specific personalities
- **High Performance** – Computational abilities open new possibilities for measurement and data processing speed
- **True Parallelism** – Enables parallel tasks and pipelining, reducing test times

FPGA-based RF Applications

Speeding up PA Power Leveling

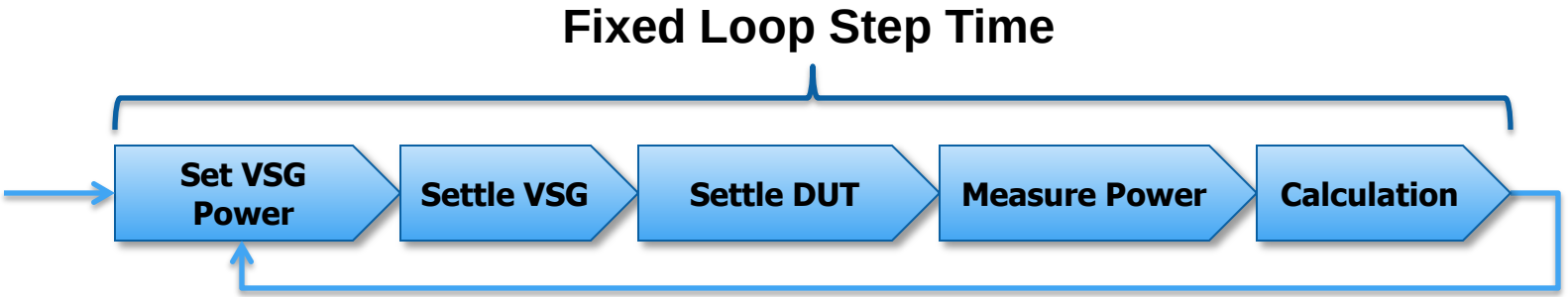
Traditional RF PA Servoing Application

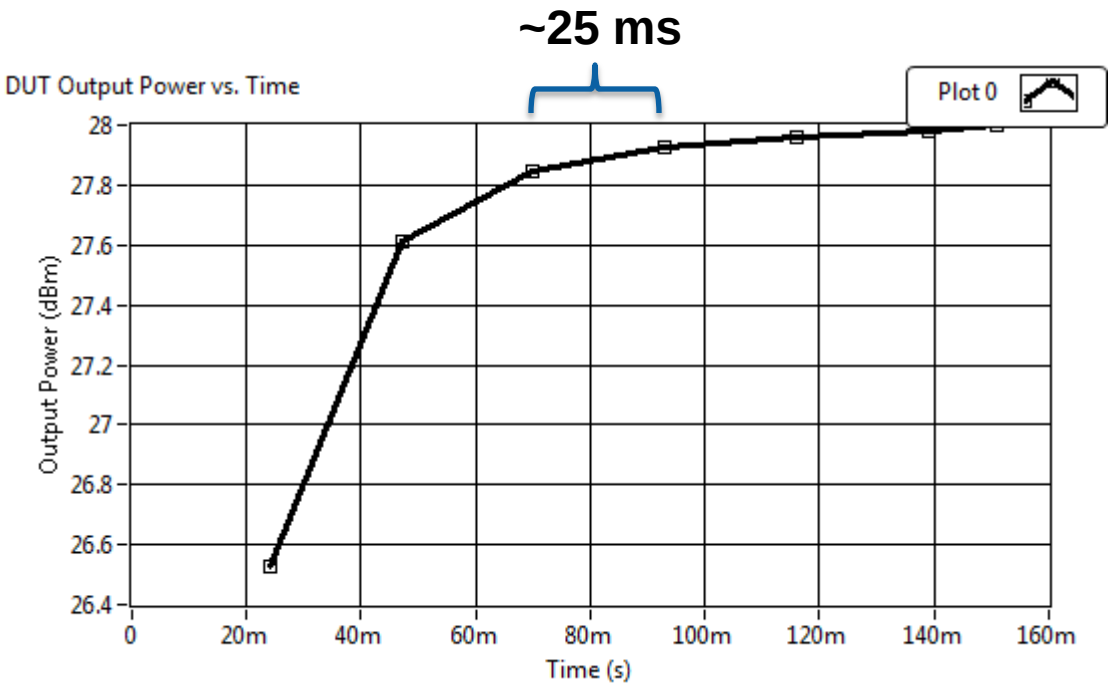


Traditional Power Leveling Loop

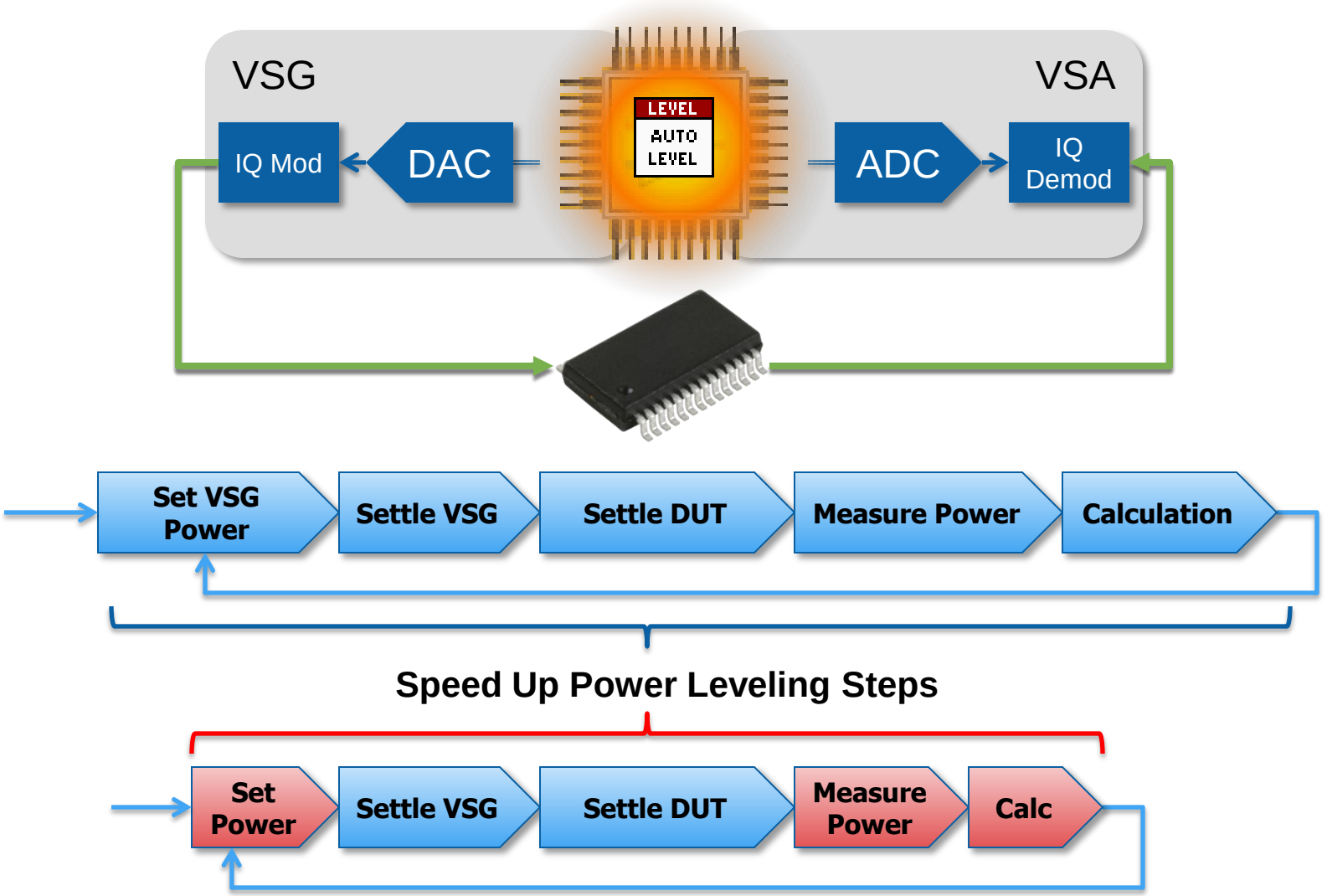
1. Pick a starting VSG power level, based on the estimated gain of the DUT.
2. Set the VSG power level.
3. Wait for the VSG to settle (amplifier & attenuator stages, switches)
4. Wait for the DUT to settle.
5. Take a measurement with the VSA.
6. If power is in range, exit.
7. If it is not, compute the new VSG power level and return to step 2.

Traditional Power Leveling Loop



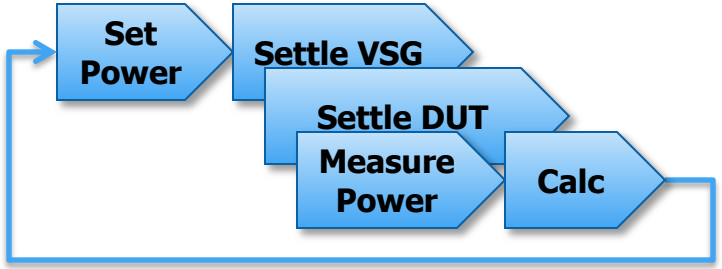


FPGA-based Power Leveling Loop

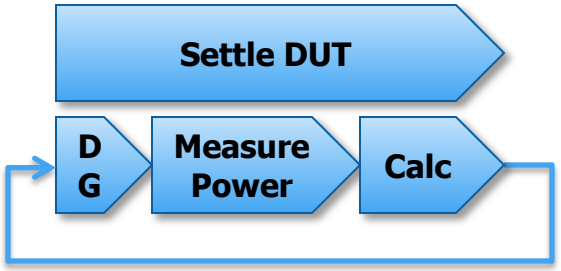


Further Speed Up Improvements

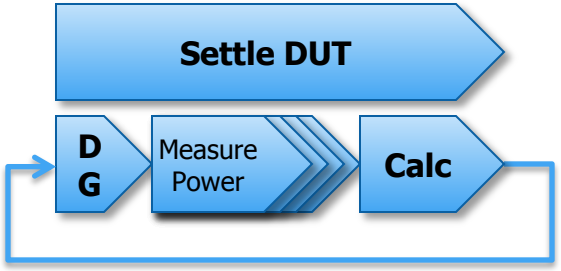
- Execute Steps in Parallel
  - Loop step time reduced but more steps required
  - Error in power measurements will reduce while converging



- Use I/Q Digital Gain (DG) control
  - VSG Output Power Stage is set only once (VSG Settling time required only once)

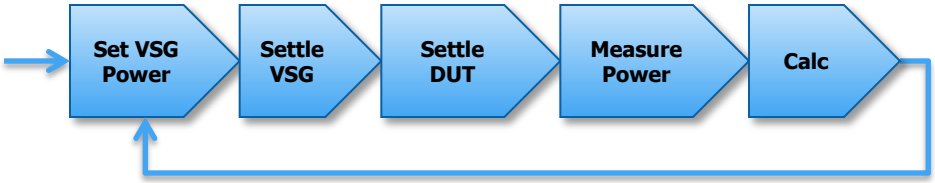


- Use Averaging Schedule
  - Reduce averaging for initial steps (faster measurement)
  - Increase averaging close to convergence (increased accuracy)

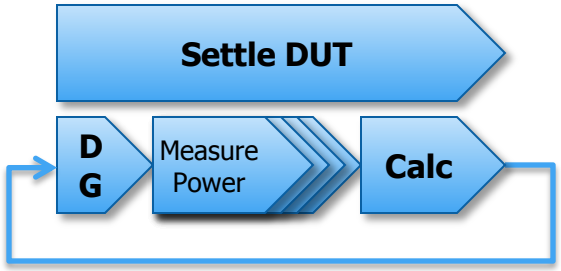


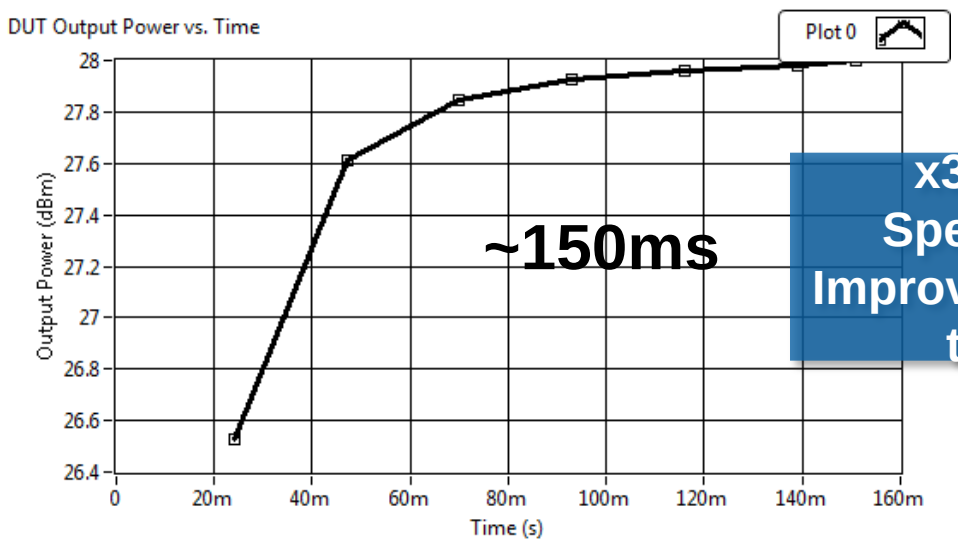
FPGA-based Power Leveling Loop

Traditional Approach



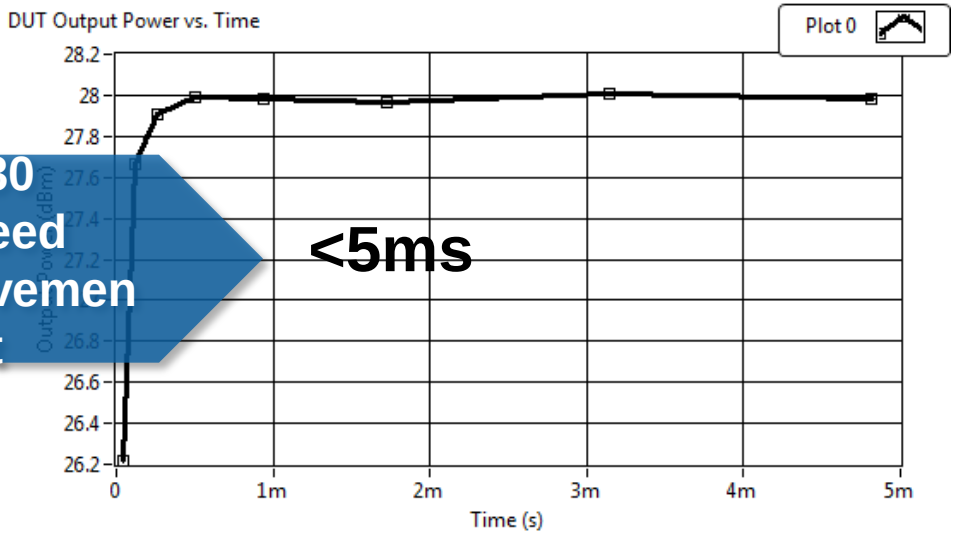
FPGA-based Optimized Approach





~150ms

x30 Speed Improvement

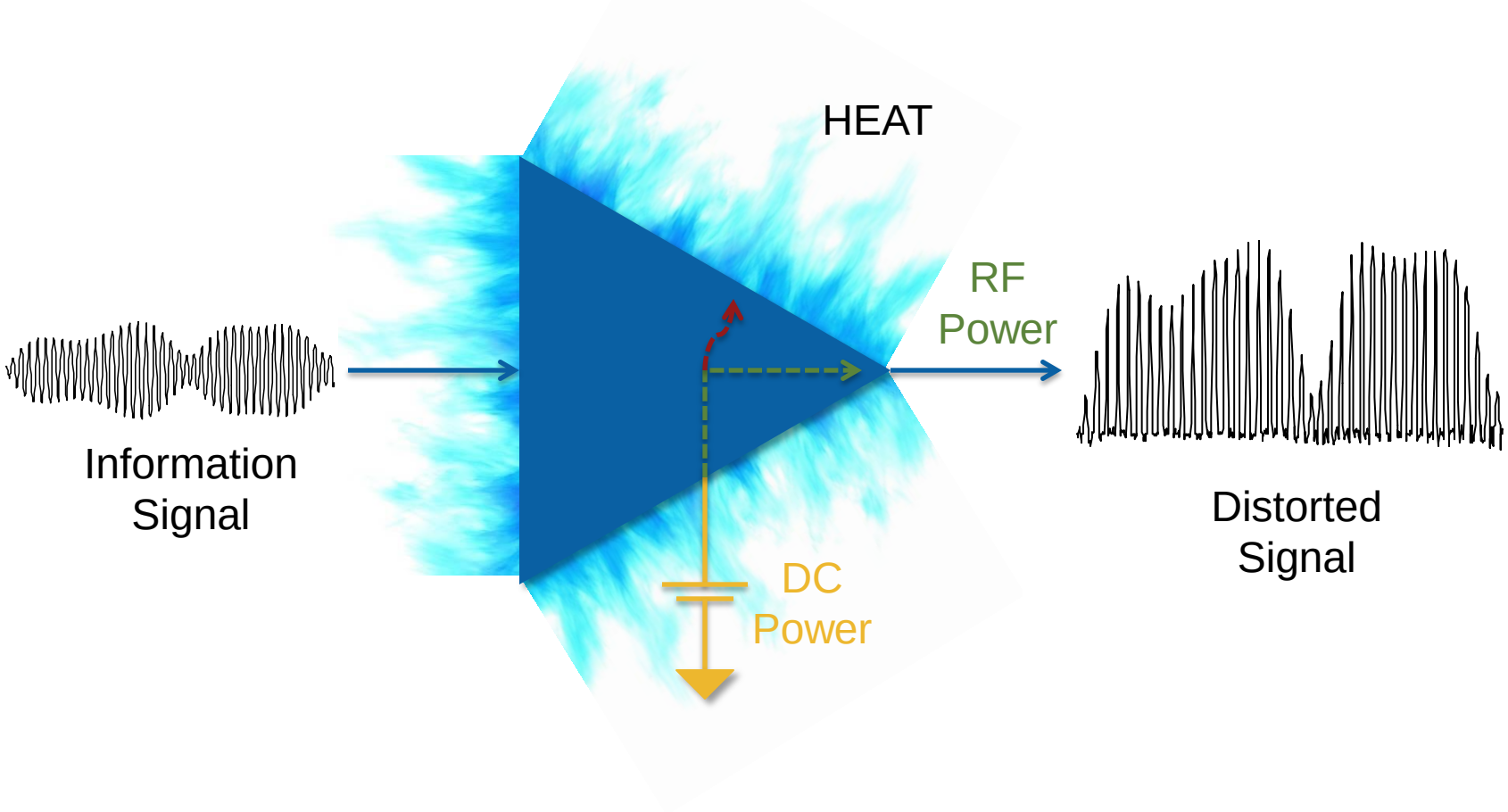


<5ms

FPGA-based RF Applications

Fast and Accurate RF Characterization under non-50 Ohm

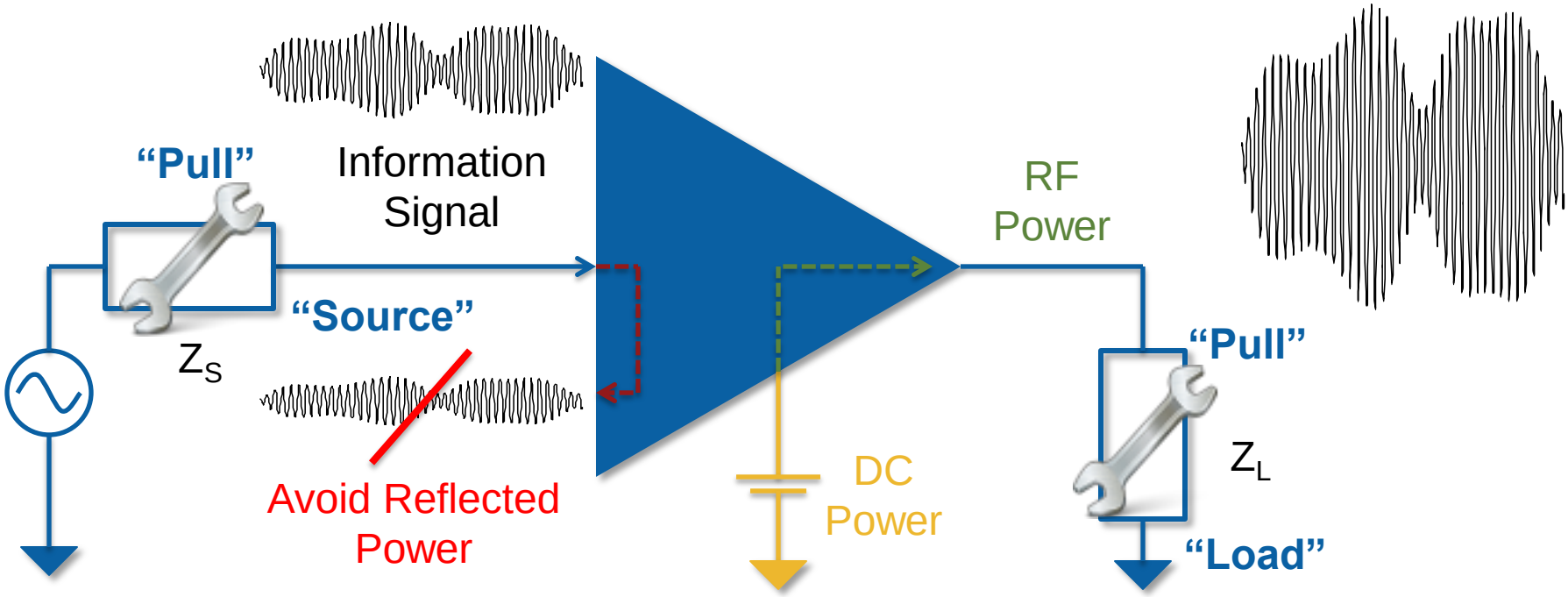
Source and Load Pull: What's all about?



How to limit power loss through heat while minimizing the signal distortion?

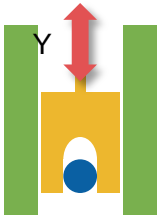
Source and Load Pull

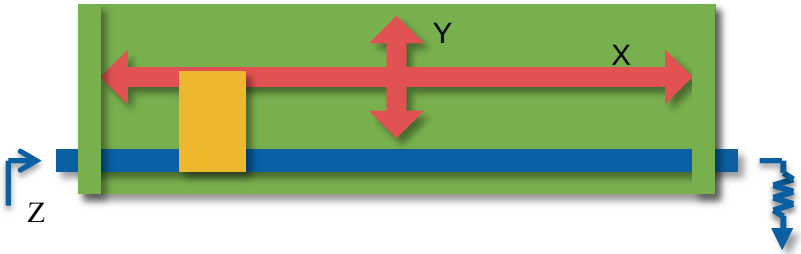
- Find the proper load impedance for optimal output power transfer with minimal distortion
- Find the proper source impedance for optimal input power transfer

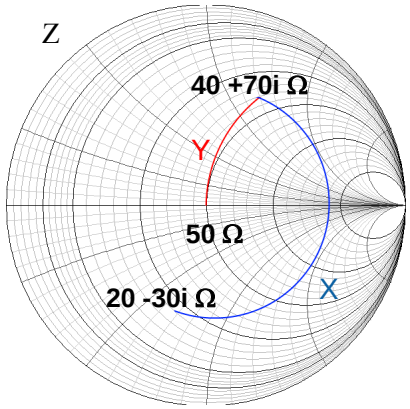


Passive Tuning Technologies

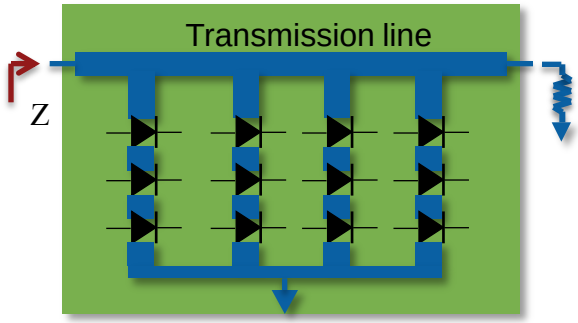
- Passive Mechanical Tuning
  - Legacy
  - Inherently support High Power
  - Using step motors (slow process)





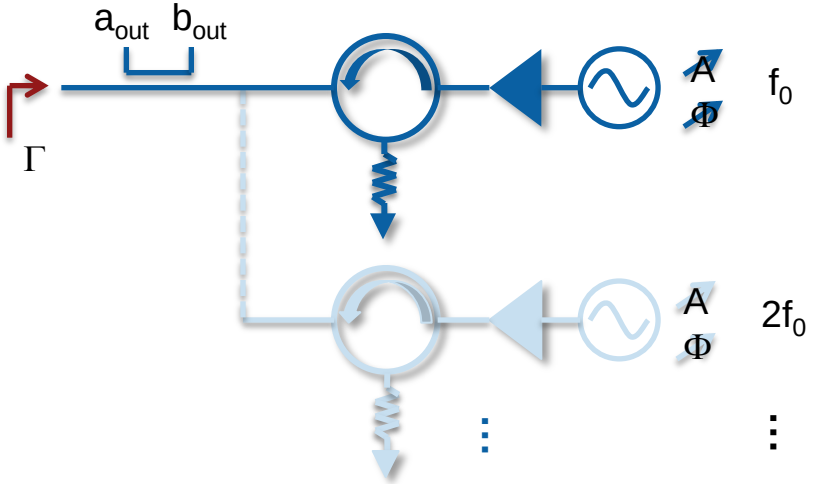


- Passive Electronic Tuning
  - Based on PIN diodes (fast)
  - Discrete set of impedances vs frequency

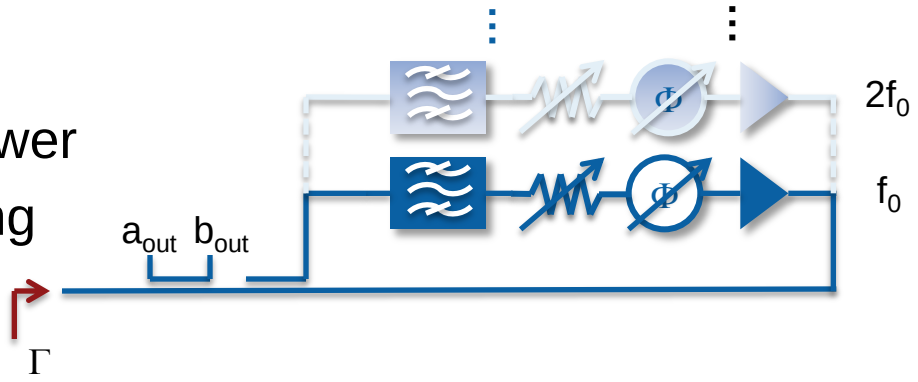


Active Tuning Technologies

- Open Loop Active Tuning
  - Very fast
  - Power Amplifier needed
  - Iterative process



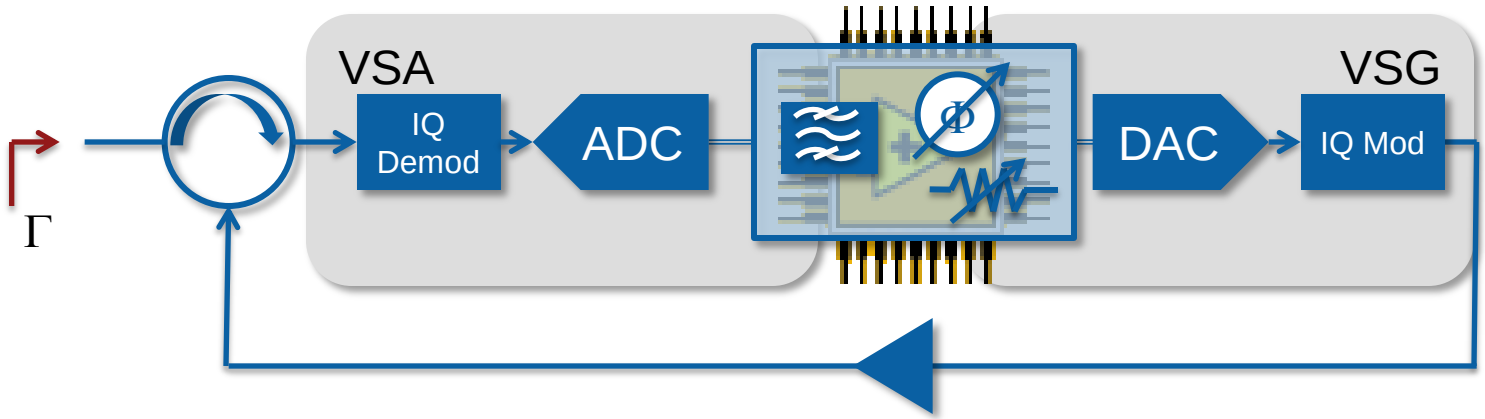
- Closed Loop Active Tuning
  - Very fast
  - Synchronized with incident power
  - Subject to oscillation depending on architecture



FPGA-based Digital Closed Loop Active Tuning

- RF signal downconverted to LF
- Continuous control of phase and amplitude
- Bandwidth and power control avoid oscillation

Pseudo-closed loop active tuning



Summary

- RF applications become more complex
  - Rapidly changing RF Standards
  - More RF Complexity in Mobile Devices
  - Increasing Test Time

- RF Instrumentation with user-reconfigurable FPGA brings significant speed and flexibility advantages

Thank you

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